## **EAST Search History**

Ref	Hits	Search Ouery	DBs	Default	Plurals	Time Stamp
#				Operator		
<u> </u>	4	(("6146908") or ("6480013")).PN.	US-PGPUB; USPAT; USOCR; EPO; IPO; DERWENT ; IBM_TDB	OR	OFF	2006/02/28 08:05
	0	(324/601.ccls.) and @ad<"20030923" and @pd>"20051202"	_	OR	NO	2006/02/28 09:59
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L7	. 27	(702/57,65,91,117,168.ccls.) and @ad<"20030923" and @pd>"20051202"	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	NO .	2006/02/28 10:17

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## **EAST Search History**

ON 2006/02/28 10:21	ON 2006/02/28 10:22	ON 2006/02/28 10:23	ON 2006/02/28 10:27	ON 2006/02/28 10:38	ON 2006/02/28 10:43	ON 2006/02/28 10:47
OR	OR	OR	OR	OR	OR	OR
US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	US-PGPUB; USPAT; EPO; IPO; DERWENT ; IBM_TDB	USPAT; USPAT; EPO; IPO; DERWENT ; IBM_TDB	US-PGPUB; USPAT; EPO; IPO; DERWENT ; IBM_TDB	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	US-PGPUB; USPAT; EPO; JPO; DERWENT ; BM_TDB
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61	1	Ξ .	20	54	. 28	<i>r</i> 0
F8	67	L10	5	L12	L13	L14

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## **EAST Search History**

7	(174/52.4.ccls.) and @ad<"20030923" and @pd>"20051202"	US-PGPUB;	OR	NO	2006/02/28 10:48
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	(((oscill\$7 VNA (vector adj network adj anal\$5)) near3 calibrat\$5) and (thru\$8 through) and probe and contact\$3 and first and second and (substrate core) and impedance and standard and (side surface link connect\$3) and (substrate material \$5film coat\$3 layer sheet pad wafer film lamina level plane circuit)).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	NO	2006/02/28 11:53
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	(((oscill\$7 VNA (vector adj network adj anal\$5)) and calibrat\$5 and (thru\$8 through) and probe and contact\$3 and first and second and (substrate core) and impedance and standard and (side surface link connect\$3) and (substrate material \$5film coat\$3 layer sheet pad wafer film lamina level plane circuit))).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	NO .	2006/02/28 12:04
	(((oscill\$7 VNA (vector adj network adj anal\$5)) and calibrat\$5 and (thru\$8 through) and contact\$3 and first and second and (substrate core) and impedance and standard and (side surface link connect\$3) and (substrate material \$5film coat\$3 layer sheet pad wafer film lamina level plane circuit)).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	SO.	NO	2006/02/28 12:22